AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus for clock stabilization detection for hardware simulation, comprising:

a digital clock module for receiving an input clock signal and a feedback clock signal and for providing an output clock signal, the digital clock module configured to lock the feedback clock signal relative to the input clock signal and configured to produce a least common multiple (LCM) clock signal and a lock signal;

a state machine for receiving the lock signal and the LCM clock signal and configured to change state of ~~deassert and assert~~ a control signal at least partially responsive to the LCM clock signal and the lock signal; and

a select circuit for receiving the control signal and the output clock signal and configured to mask application of the output clock signal responsive to a first state ~~deassertion~~ of the control signal and to unmask the application of the output clock signal after the output clock signal is sufficiently stabilized as indicated by a second state ~~assertion~~ of the control signal by the state machine for the hardware simulation to commence.

2. (Original) An apparatus, as in claim 1, further comprising a buffer coupled to receive the output clock signal and to provide the feedback clock signal, the output clock signal generated responsive to the input clock signal.

3. (Original) An apparatus, as in claim 1, wherein the feedback clock signal is the LCM clock signal.

4. (Original) An apparatus, as in claim 1, wherein the digital clock module is disposed in a programmable logic device (PLD), and wherein the PLD comprises a configuration logic block configured with the state machine.

5. (Original) An apparatus, as in claim 1, wherein the state machine is a register.

6. (Original) An apparatus, as in claim 1, wherein the control signal is configured to cause the select circuit to pass the output clock signal for at least approximate edge coincidence with another output clock signal.

7. (Original) An apparatus, as in claim 1, wherein the state machine comprises an edge detector configured to detect at least proximal phase alignment between the LCM clock signal and the output clock signal to provide the control signal.

8. (Currently Amended) A method for clock stabilization detection for hardware simulation, comprising:

receiving an input clock signal;

producing a feedback clock signal from the input clock signal;

producing an output clock signal from the input clock signal;

locking the feedback clock signal relative to the input clock signal to produce a lock signal;

generating a least common multiple (LCM) clock signal;

~~deasserting and asserting~~ changing state of a control signal at least partially responsive to the LCM clock signal and the lock signal; and

masking application of the output clock signal responsive to a first state ~~deassertion~~ of the control signal; and

unmasking the application of the output clock signal after the output clock signal is sufficiently stabilized as indicated by a second state ~~assertion~~ of the control signal for the hardware simulation to commence.

9. (Original) A method, as in claim 8, further comprising detecting at least proximal phase alignment between the output clock signal and the LCM clock signal to generate the control signal.

10. (Original) A method, as in claim 8, wherein the masking further masks application of the LCM clock signal responsive to the control signal.

Claims 11-13. (Cancelled)

14. (Currently Amended) An apparatus for clock stabilization detection for hardware simulation, comprising:

a digital clock module for receiving an input clock signal, the digital clock module configured to produce a plurality of output clock signals at least partially responsive to the input clock, one of the plurality of output clock signals being fed back to the digital clock module as a feedback clock signal to establish lock with the input clock signal, the digital clock module configured to produce a least common multiple (LCM) clock signal for and as part of the plurality of output clock signals, the digital clock module configured to produce a lock signal responsive to establishment of the lock;

a state machine for receiving the lock signal and the LCM clock signal and configured to change state of ~~deassert and assert~~ a control signal partially responsive to the LCM clock signal and the lock signal, the state machine including an edge detector for receiving the plurality of clock signals, the edge detector configured to detect at least proximal phase alignment of all the plurality of clock signals to produce the control signal; and

select circuits for receiving the control signal and respectively receiving the plurality of clock signals, each of the select circuits configured to mask application of a respective one of the plurality of output clock signals responsive to a first state ~~deassertion~~ of the control signal and to unmask the application of the plurality of output clock signals after sufficiently stabilized as indicated by a second state ~~assertion~~ of the control signal for the hardware simulation to commence.

15. (Original) An apparatus, as in claim 14, wherein the lock is a frequency lock, and wherein the at least proximal phase alignment is to a rising edge for all of the plurality of clock signals.

16. (Original) An apparatus, as in claim 14, wherein the select circuits are multiplexers.

17. (Original) An apparatus, as in claim 16, wherein each of the multiplexers have one input terminal coupled to receive the respective one of the plurality of output clock signals and another input terminal coupled to electrical ground.

18. (Original) An apparatus, as in claim 14, wherein the digital clock module is part of a field programmable gate array (FPGA) integrated circuit.

19. (Original) An apparatus, as in claim 18, wherein the state machine is configured in the FPGA integrated circuit with configurable logic.

20. (Original) An apparatus, as in claim 19, wherein the LCM clock signal and feedback clock signal are sent to respective buffers prior to being input to the state machine and the digital clock module, respectively.

21. (Original) An apparatus, as in claim 20, wherein the buffers are multiplexers configured for buffering.

22. (Original) An apparatus, as in claim 14, wherein the state machine comprises a register.

23. (Original) An apparatus, as in claim 14, wherein the state machine is configured to produce another control signal for adjusting phase, the other control signal provided to the digital clock module for phase adjustment of at least one of the plurality of output clock signals.

24. (Currently Amended) A test system for clock stabilization detection for hardware simulation of an integrated circuit, comprising:

a computer having a processor, an input/output interface and memory, the memory for storing target test results and a test program, the input/output interface for communicating with the integrated circuit;

a clock source for providing an input clock signal to the integrated circuit;

the integrated circuit configured with a clock stabilization circuit, the clock stabilization circuit configured to:

produce a feedback clock signal from the input clock signal;

produce an output clock signal from the input clock signal;

lock the feedback clock signal relative to the input clock signal to produce a lock signal indication of the lock;

generate a least common multiple (LCM) clock signal;

~~deassert~~ change state of a control signal to a first state partially responsive to the LCM clock signal and the lock signal;

detect at least proximal phase alignment between the LCM clock signal and the output clock signal for ~~assertion~~ changing state of the control signal to a second state;

selectively apply the output clock signal to a design portion of the integrated circuit responsive to the control signal, the control signal selecting application of the output clock signal to the design portion after the lock and after detection of the at least proximal phase alignment of the LCM clock signal and the output clock signal; and

mask application of the output clock signal until the output clock signal is sufficiently stabilized as indicated by ~~assertion of~~ the control signal being in the

second state for the hardware simulation to commence; and

the test program configured to cause test vectors to be applied responsive to ~~assertion~~ the second state of the control signal, the test vectors applied to the design portion to obtain test results from the integrated circuit.

25. (Original) A test system, as in claim 24, where selective application of the output clock signal is done for at least approximate edge coincidence with another output clock signal.

26. (Original) A test system, as in claim 24, where selective application of the output clock signal is done for staggered edges with respect to another output clock signal.

27. (Currently Amended) A test system for clock stabilization detection for hardware simulation of an integrated circuit, comprising:

a computer having a processor, an input/output interface and memory, the memory for storing target test results and a test program, the input/output interface for communicating with the integrated circuit;

a clock source for providing an input clock signal to the integrated circuit;

the integrated circuit configured with a first portion of a clock stabilization design, the computer instantiated with a second portion of the clock stabilization design;

the first portion of the clock stabilization design configured to:

produce a feedback clock signal from the input clock signal;

produce an output clock signal from the input clock signal;

lock the feedback clock signal relative to the input clock signal to produce a lock signal indication of the lock; and

generate a least common multiple (LCM) clock signal;

the second portion of the clock stabilization design configured to:

change state of ~~deassert and assert~~ a control signal partially responsive to the LCM clock signal and the lock signal; and

detect at least proximal phase alignment between the LCM clock signal and the output clock signal for changing a state ~~assertion~~ of the control signal;

the first portion of the clock stabilization design coupled to receive the control signal and configured to selectively apply the output clock signal to a design portion of the integrated circuit responsive to changing the state ~~assertion~~ of the control signal;

the first portion of the clock stabilization design responsive to ~~assertion~~ changing the state of the control signal selecting application of the output clock signal to the design portion after the lock and after detection of the at least proximal phase alignment of the LCM clock signal and the output clock signal;

the application of the output clock signal being masked until the output clock signal is sufficiently stabilized as indicated by the second portion of the clock stabilization design changing the state of ~~asserting~~ the control signal for the hardware simulation of the design potion to begin; and

the test program configured to cause test vectors to be applied responsive to changing the state ~~assertion~~ of the control signal, the test vectors applied to the design portion to obtain test results from the integrated circuit.